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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/216,078	12/18/98	NI C	016517-00380

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MMC2/0913

EXAMINER	
GARCIA, J	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/13/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/216,078	Hsinchu et al
Examiner	Group Art Unit
Joannie Adelle Garcia	2823

☒ Responsive to communication(s) filed on 6/26/00

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claim

☒ Claim(s) 1-28 is/are pending in the applicat

Of the above, claim(s) 1 and 17-19 is/are withdrawn from consideration

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 2-16 and 20-28 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☒ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

The indicated allowability of claims 2-4, 6, 9, 11-16, and 21 is withdrawn in view of the newly discovered reference to Grider et al. Rejections based on the newly cited reference(s) follow.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

Claims 2-9, and 20-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Grider et al (U.S. Patent 6,093,659).

Grider et al teaches providing a semiconductor substrate 30 having a first region where a first oxide layer thickness is desired and a second region where a second oxide layer thickness is desired, forming a gate dielectric layer 34 comprising an oxide layer overlying said semiconductor substrate including said first region and said second region, introducing a halogen-containing impurities by an ion implantation process into said semiconductor substrate to form a higher halogen concentration in said first region than in said second region, performing an oxidizing process on said semiconductor substrate to simultaneously form said first oxide layer thickness 20 at said first region and said second oxide layer thickness 22 at said second region, and forming a first memory gate electrode 16 on said second oxide layer, said second oxide layer thickness

formed on said semiconductor substrate in a memory region. He is also teaching that introducing said halogen-containing impurities comprises masking said gate dielectric layer to expose said first region, said dielectric layer formed on said substrate, and wherein said halogen-containing impurities are introduced through said dielectric to said first region. He discloses as well, that introducing said halogen-containing impurities comprises introducing halogen-containing into said first region and wherein said second region has substantially no halogen concentration therein. He is also disclosing that said halogen-containing impurities are selected from fluorine bearing impurities, chlorine bearing impurities, bromine bearing impurities, and iodine bearing impurities. Grider et al discloses the suitability of implanting halogen ions into the "first region", at a different concentration to achieve desired gate oxide thicknesses. Grider et al is also teaching providing a semiconductor substrate 30, said semiconductor substrate comprising a memory cell region, a first region for a MOS transistor, and a second region for a high voltage device. (Figures 1-5, Column 3, lines 14-16, 21-26, 49-53, and 62-67, Column 4, lines 1, 8-11, and 19-25)

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grider et al as applied to claims 2-9, and 20-28 above, and further in view of the following comment.

Grider et al does not teach that said semiconductor device comprises a flash EEPROM semiconductor device. However, a substrate produced would be suitable as a substrate for formation of a flash EPROM semiconductor device.

Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grider et al as applied to claims 2-9, and 20-28 above, and further in view of the following comments.

Grider et al discloses forming core logic of a memory cell array over one of the gate oxide regions and peripheral circuitry at another of the gate oxide regions (Column 1, lines 16-21). The examiner takes judicial notice that the particular gate formation steps of claims 11-16 were known to be suitable at the time of applicant's invention in formation of core logic and/or peripheral circuitry of a memory array. It would have been within the scope of one of ordinary skill in the art to employ the prior art process for it's disclosed intended purpose to achieve the formation step of a memory cell array of Girder et al.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group Receptionist whose telephone number is (703) 308-0956. **See MPEP 203.08.**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner J. Garcia whose telephone number is (703) 306-5733. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax number for this group is (703)308-7722(and 7724 and 7382). MPEP 502.01 contains instructions regarding procedures used in submitting responses by facsimile transmission.

George Fourson
Primary Examiner
Art Unit 2823

JAG
September 6, 2000